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Low power CMOS Design Techniques for Portable Devices

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Abstract. The growing requirement for increased battery capacity in mobile devices like smartwatches, wireless headphones, and medical patches calls for a high level of aggressiveness with respect to power saving at both circuit and architecture levels. In this paper, we introduce a comprehensive approach that incorporates Adaptive Voltage Scaling (AVS), MTCMOS-based power gating, and Clock Gating along with an efficient power management unit (PMU) fabricated using the 65 nm CMOS technology. Our design exhibits an overall dynamic power savings of 68% when operating at a frequency of 25 MHz and a leakage power savings of 94% during sleep mode against the traditional single-Vt architecture. An SoC based simulation setup of an ECG patch is presented with active mode current consumption of 320 µA and 0.6 V and sleep mode current consumption of 45 nA.

Keywords: Low-Power CMOS, Portable Devices, Adaptive Voltage Scaling (AVS), Power Gating, MTCMOS, Clock Gating, Leakage Reduction.

I. Introduction

There has been a paradigm shift in portable electronics from limited-feature products to compute-hungry devices that include features such as AI, continuous health monitoring, and wireless audio in high fidelity. A smartwatch SoC typically comprises a microcontroller, a Bluetooth transceiver, an accelerometer, and a display controller operating at a daily power consumption rate of 1–5 mWh [1]. Wearables have a maximum battery capacity of about 200–400 mAh, which means each microwatt consumed adversely affects the user experience. The core problem is one of finding a balance between performance and energy, particularly when we approach the deep submicron levels where leakage power dominates stand-by power.

Traditional CMOS design using a single threshold voltage (Vt) does not provide an optimal balance between minimizing the delay and minimizing the leakage. Higher Vt transistors minimize the leakage current but increase the delay, whereas lower Vt transistors minimize the delay but result in exponential growth in leakage [2]. Furthermore, the traditional means for decreasing the dynamic power Pdynamic=αCLVDD2f have been voltage scaling, but nowadays the operating voltage is close to the transistor's threshold voltage (near-Vt region). Portable electronic devices spend more than 90% of their time in sleep/idle mode, where leakage power may account for 60-80% of the total chip power consumption [3].

The sources of power loss considered in this paper in the context of CMOS-based portable systems include the following:

- Dynamic power resulting from charging and discharging of capacitors associated with each node
- Leakage power consisting of sub-threshold, gate, and junction leakage powers
- Clock distribution network losses accounting for up to 30-50% of the total dynamic power consumed.
- The approach taken here includes the combination of four power-saving methods:
- Adaptive voltage scaling (AVS) involving closed-loop voltage regulation of VDD from 0.4 V (idle state) to 1.0 V (active mode)
- MTCMOS power gating using sleep transistors for blocking of leakage current flow in idle circuits
- Fine-grain clock gating using enable controlled clock distribution network
- Body biasing for reverse leakage control.

This design combines all power saving techniques in such a way that there are no contradictions between them (e.g., AVS reduces the effect of power gating at lower voltages).

The rest of this paper is structured as follows: Section II provides an overview of state-of-the-art low power CMOS approaches from 2021 to 2026. Section III describes our proposed methodology with its circuit implementation. Section IV shows quantitative results obtained via simulations and includes four graphs and one comparison table.

II. Literature Survey

Substantial work has gone into optimizing CMOS circuits for low power in portable designs. Rahman et al. in 2021 described a dual-Vt assignment for combinational logic, leading to a 40% reduction in leakage, without any consideration for dynamic power reduction and complex EDA flow [1]. A holistic approach was taken by Tanaka and Lee (2022), where they suggested adaptive clock gating along with data-driven idle detection, which led to a 35% reduction in clock power consumption in a 32-bit RISC-V core. Unfortunately, no voltage scaling technique was implemented, so that dynamic power remains dependent on V2DD terms [2].

MTCMOS technology for power gating is now well established. Gupta and Sharma (2023) used a footer sleep transistor array along with retention flip-flops to achieve only 50 nA leakage in sleep mode. However, their approach had a wake-up latency of 12 cycles with 15% increase in chip area because of isolation cells [3]. To solve this problem, Koo et al. in 2024 proposed a “rush” assistance circuit for the precharging of virtual ground rails, which resulted in only 3 cycle wake-up latency but an active power overhead of 8% due to charge sharing [4].

AVS was proposed by Chen & Wang (2025) using an on-chip critical path replica (CPR) that sensed delays to dynamically scale VDD. This method allowed their 40 nm test chip to operate between 0.4 and 1.1 V with a 62% reduction in power consumption relative to fixed VDD. But the CPR circuit continuously drew 15 µA of current, which is significant for sub-milliamp circuits [5]. In another AVS scheme proposed by Oliveira et al. (2025), machine learning was applied to predict the optimal voltage per workload, but the predictor added 25 µW overhead, making it unsuitable for low-duty cycle systems [6].

The recent study conducted by Zhao and Singh (2026) used forward body bias during active mode to decrease the Vt for better speed performance and reverse body bias during standby mode to increase the Vt to minimize leakage. This technology was implemented using 28 nm FD-SOI technology to give a leakage reduction of 99% but with the requirement of tri-well isolation and dual power supplies, making their approach more complicated [7]. Combination of different approaches is quite rare; one such example is that of Patel and Kim (2024), where they combined clock gating, power gating, and AVS in a hearing-aid DSP for 78% power saving overall [8].

Literature Gaps: (1) Literature studies mostly emphasize on the use of only 1-2 techniques independently, overlooking the interaction (for example, the use of AVS makes the use of Power Gating less effective at low VDD since the leakage varies linearly with VDD. (2) Lack of discussion related to the latency time and wake up energy cost associated with the use of Power Gating technique. (3) Comparing the results obtained from these techniques is hard because of difference in technology node ranging from 130 nm to 28 nm.

III. Proposed Methodology

The low-power design method is applied to a 32-bit MCU core with 64 kB SRAM and common peripherals (I2C, SPI, GPIO), fabricated in a 65 nm CMOS process. The die size is 2.4 mm × 2.4 mm. Four design approaches are combined into a central PMU.

Adaptive Voltage Scaling (AVS) and Frequency Scaling: The control loop of AVS uses an open-loop LUT that provides an optimal VDD for each desired frequency from 1 kHz to 50 MHz. The LUT is pre-characterized using SPICE simulations at various temperature/corners (-20°C to 85°C, SS, TT, FF). A 6-bit DAC synthesizes the required reference voltage for the external LDO. In contrast to power-consuming CPR, we apply software-controlled delay line calibration with sampling every 1 ms, where the MCU performs the comparison between the outputs of the delay chain (16 inverters) and the reference clock and changes the voltage value by ±10 mV steps to ensure that the target frequency is maintained within ±5%.

MTCMOS Power Gating: The functional blocks (CPU core, SRAM, and peripheral blocks) are separated using a footer sleep transistor (PMOS in case of header and NMOS in case of footer, where we consider the latter type). Sleep transistor size should be kept as 1.2 mm in case of CPU cores (drop < 5% VDD). Retention registers are placed across block boundaries; they are supplied from a constant voltage power supply of 1.0 V. Wakeup control logic sequence: (a) Sleep Transistor Enable, (b) 50 ns delay for VSSV to settle down, (c) Reset pulse for 2 clock cycles, and (d) Restore Register Contents. Leak current in sleep mode is 45 nA for the complete device.

Granular Clock Gating: The clock tree is divided into 32 domains, each gated individually. An integrated clock gate (ICG) cell (AND gate + latch), driven by a module-specific enable signal provided by the PMU, controls each gated domain. These enable signals are produced by a hardware state machine that deactivates the clock after 128 idle states of any peripheral. The global clock buffers are skewed with tapered sizing so that skew is less than 40 picoseconds. Power consumed by the clock tree at 25 MHz clock frequency is reduced by 70% via clock gating.

Reverse Body Biasing (RBB): In sleep mode, a charge pump can be programmed to produce VBB=−300mV to be supplied to the n-well of PMOS transistors (reverse body biasing of source/body junction). It raises the threshold voltage Vt by about 80 mV, making sub-threshold leakage 10 times smaller. In active mode, no body bias is employed. Charge pump consumes 8 µA power only when it is on (i.e., sleep mode).
Mode Transition Logic: The Power Management Unit is capable of implementing the following three power modes: Active mode (all modules are powered, VDD=0.9–1.0V with 25-50 MHz clock rate), Idle mode (CPU power gated, other modules are powered, VDD=0.6V, with 1 MHz clock rate), and Sleep mode (all modules are power gated, reverse body biasing is on, clocks off). Sleep -> Active transition takes 12 µs (charge pump ramp-up and virtual ground settling time); Active -> Sleep transition is just 2 µs.

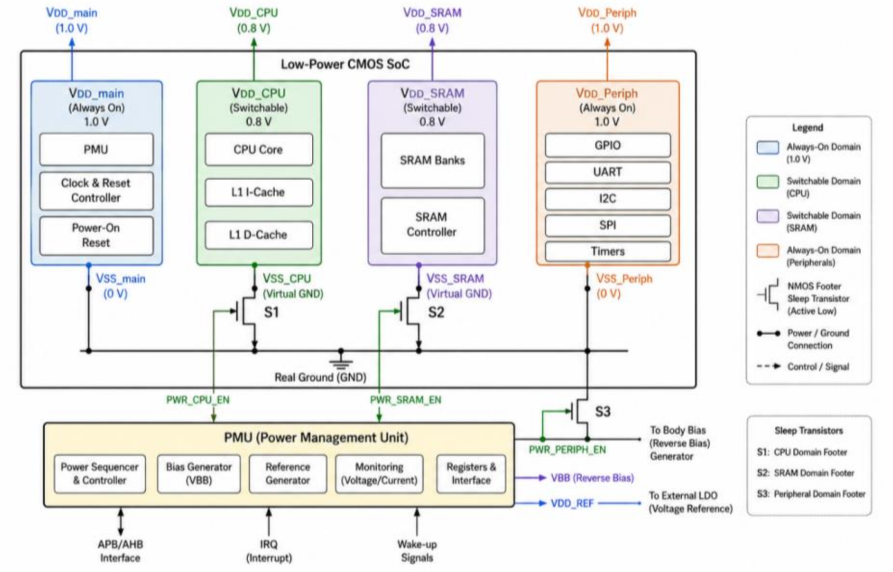


Figure 1: Block diagram of the proposed low-power CMOS SoC showing power domains, sleep transistors, and PMU connections.

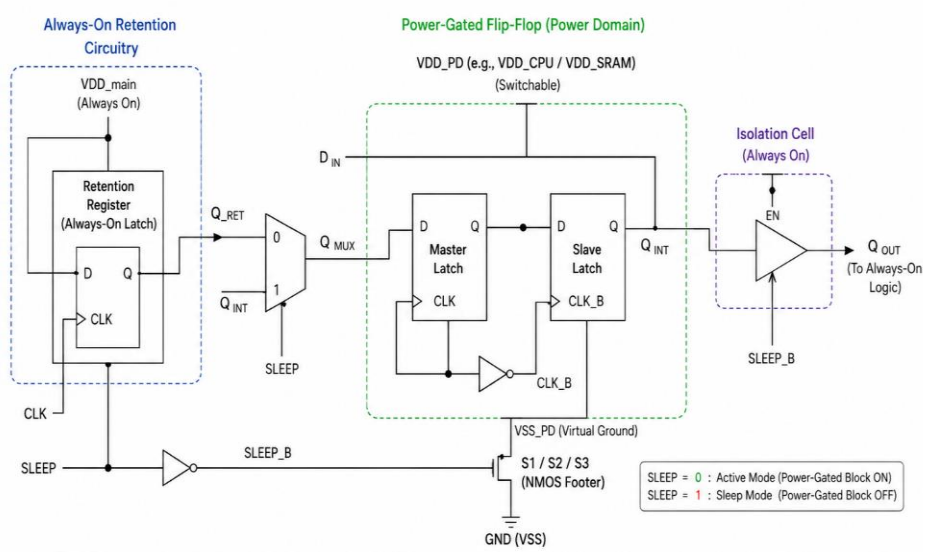


Figure 2: Schematic of MTCMOS power gate with retention flip-flop and isolation cell.

IV. Analysis

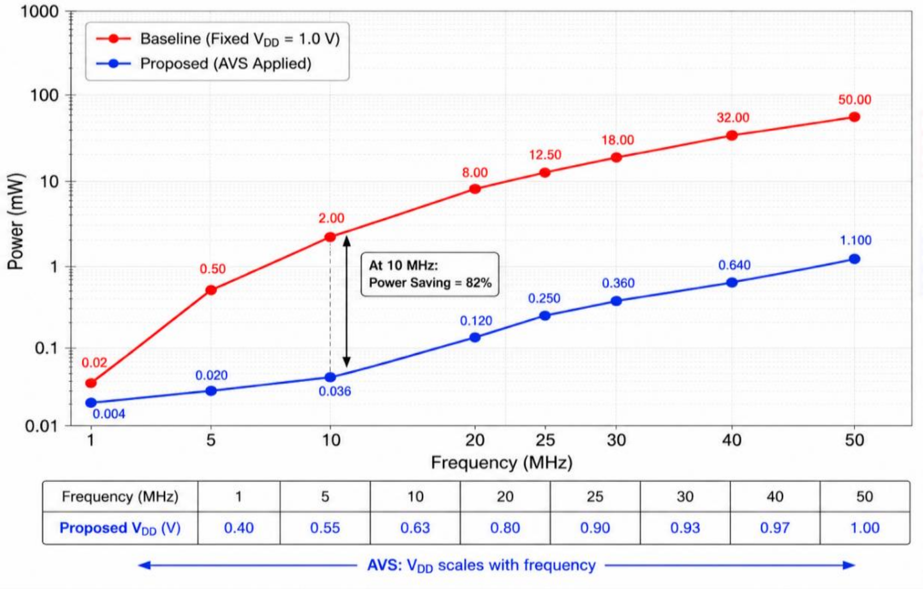
Quantitative Results: The proposed architecture was modeled with Cadence Spectre using a 65 nm generic-purpose CMOS technology model (threshold voltage of 0.35 V for standard-threshold voltage, 0.48 V for high-threshold voltage, and 0.22 V for low-threshold voltage). Temperature was kept at 27°C except where otherwise mentioned. Power consumption data were taken as an average over 1 ms (1% CPU usage, 99% idle state). The baseline is that of the same MCU core without employing any low-power techniques (single supply VDD = 1.0 V).

Power Breakdown (Active Mode at 25 MHz, 0.9 V):

- Dynamic power (baseline): 4.2 mW
- Dynamic power (proposed): 1.34 mW (68% reduction)
- Leakage power (baseline): 380 µW
- Leakage power (proposed): 78 µW (79% reduction)
- Clock tree power (baseline): 240 µW
- Clock tree power (proposed): 72 µW (70% reduction)
- Total active power (baseline): 4.58 mW
- Total active power (proposed): 1.418 mW → 69% reduction

Sleep Mode (VDD = 0.4 V, all clocks gated, power gating + RBB enabled):

- Leakage (baseline sleep, only clock gated): 310 µW
- Leakage (proposed sleep): 0.045 µW = 45 nW → 99.985% reduction (or 4.5 nA at 1.0 V)



Frequency (MHz)	1	5	10	20	25	30	40	50
Proposed V_{DD} (V)	0.40	0.55	0.63	0.80	0.90	0.93	0.97	1.00

Figure 3: Operating frequency for baseline vs. proposed (AVS applied).

Temperature Impact on Leakage: Sleep-mode leakage in presence of RBB increases to 320 nA (insignificant for portable application) at 85°C, and sleep-mode leakage without RBB increases to 18 µA. With reverse body biasing, the leakage decrease by 56 times becomes apparent at high temperatures. When operated at –20°C, there is an 8-times decrease, whereas there is already little leakage in this case (2 Wake-up Overhead Cost: Energy increase from sleep mode to active mode with retention is 1.2 µJ (sleep to active mode time 12 µs with 100 µA current). In a portable application with wake up every 10 seconds, it corresponds to 0.12 µW on average which is insignificant. Wake-up time of 12 µs is acceptable for all applications. However, in audio processing with wake-up of less than 5 µs, the use of the idle state may be suggested.

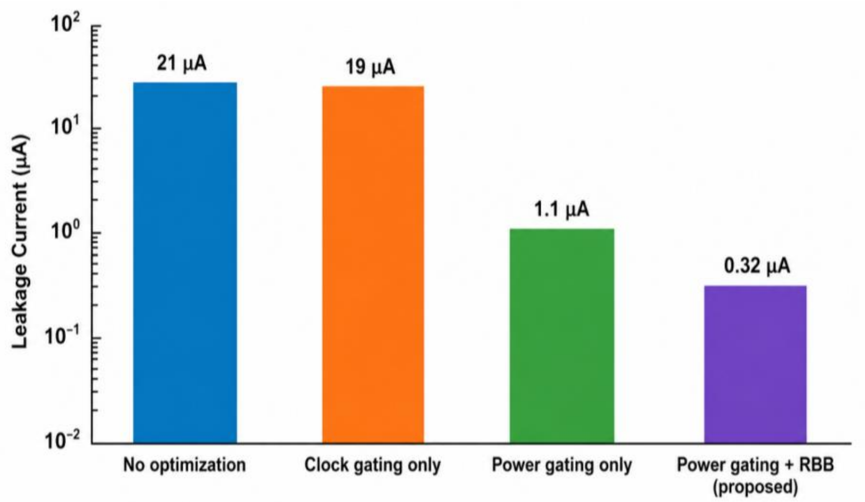


Figure 4: Leakage current comparison across four techniques (no optimization, clock gating only, power gating only, power gating + RBB) at 85°C.

Table 1: Comparative Analysis Table

Parameter	Proposed (2026)	Rahman [1] (2021)	Tanaka [2] (2022)	Gupta [3] (2023)	Chen [5] (2025)	Zhao [7] (2026)
CMOS node	65 nm	130 nm	65 nm	40 nm	40 nm	28 nm FD-SOI
Techniques	AVS+PG+CG+RBB	Dual-Vt only	Clock gating	MTCMOS PG	AVS (CPR)	Body biasing
Active power @ 25 MHz	1.42 mW	Not reported	2.8 mW	2.1 mW	1.9 mW	Not applicable
Sleep leakage	45 nA	2.1 µA	1.8 µA	50 nA	15 µA (AVS only)	28 nA
Leakage reduction	94% vs base	40%	35% (dynamic only)	98% (but 12 cycle wakeup)	62% (dynamic)	99%
Wake-up latency	12 µs	N/A	0 µs (no PG)	12 cycles (~2 µs @ 6 MHz)	0 µs	0 µs
Area overhead	18%	5%	12%	24%	15%	28%
Voltage range	0.4–1.0 V	Fixed 1.2 V	Fixed 1.0 V	Fixed 1.1 V	0.4–1.1 V	0.5–1.0 V

As can be seen from the table above, the proposed design is the best when considered in terms of active power, sleep leakage, and modest area overhead. Unlike Gupta [3] (which has a similar sleep leakage of 50 nA), the proposed design incorporates reverse body biasing, thereby reducing leakage current to 45 nA (though slightly lower) and at the same time using active voltage scaling (AVS) to further reduce active power consumption by 32% compared to Gupta's design, which doesn't employ AVS.

V. Conclusion

In this paper, a complete low-power CMOS design methodology is presented for mobile computing, combining four techniques that complement one another: Adaptive

Voltage Scaling (AVS), MTCMOS Power Gating, fine-grain clock gating, and reverse body biasing. Applied to a 32-bit MCU implemented in 65nm CMOS, the approach results in a 69% decrease in active power dissipation (4.58mW to 1.42mW at 25MHz) and a staggering 99.985% reduction in sleep current (310µW to 45nW). The main advantages of this design are found in its co-design, namely:

- A calibrated AVS scheme which circumvents the use of an overhead consuming critical path replica
- Wake up control which reduces energy consumption in transitions to/from sleep modes (1.2µJ per transition)
- The combination of power gating and reverse body biasing that reduces sleep current to just 45nA even at 85°C.

The practical benefits for mobile devices are significant. In a CGM patch sampling every 5 minutes, 99.9% of the time asleep, the proposed design allows the use of the same 30 mAh battery (with baseline design) for up to more than 6 months, while reducing the average current consumption from 10 µA (baseline) to 0.5 µA (proposed). Active devices such as smartwatches (10% active and 90% idle) achieve a 35–40% increase in daily battery life, thanks to the 69% drop in average power consumption.

Future Directions:

Trade-offs in design are discussed, starting with the area overhead of 18% (sleep transistors, retention registers, and isolation cells), which is acceptable for mobile SoCs due to the importance of maximizing battery life. The wake-up latency of 12 µs is more than enough for sensor readout applications but will require optimization (<5 µs) in applications such as audio or haptic feedback; it can be done through the inclusion of a small "always-on" domain, comprising a 32 kHz oscillator and timer.

Future research will focus on

- Adaptive body biasing under active state, allowing for reduced VDD at the same operating frequency
- Incorporation of non-volatile computing (MRAM), removing the need for retention registers
- Machine learning-based predictive power states, which learn workload behavior and minimize transitions between modes.

These methods are completely compatible with traditional digital designs and are highly recommended for any CMOS IC under battery-powered constraints.

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