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High-Efficiency DC-DC Converter for Portable Electronics

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Abstract. In light of increasing demand for portable devices, there is an increased requirement for efficient power conversion schemes to enhance battery capacity and reduce power loss via heat dissipation. In this paper, a new hybrid DC-DC topology is presented which comprises a Switched-Capacitor (SC) block coupled with a reconfigurable interleaved buck circuit that can reach a maximum efficiency of 94.7% under a 1.8 W load. The power supply designed for battery-operated systems, powered by Li-ion batteries (2.7V-4.2V input voltage), delivers a stable 1.2V output with low quiescent current consumption of only 18 µA. The power loss evaluation is extensively covered. When compared with three modern converters designed between 2022 and 2025, the developed converter shows higher efficiency levels at lower loads (88.2% at 10mA) and reduced settling time of 6.5 µs.

Keywords: DC-DC Converter, High Efficiency, Portable Electronics, Switched-Capacitor, Interleaved Buck, Power Management IC (PMIC), Light-Load Efficiency.

I. Introduction

Modern portable devices such as wireless headphones, fitness trackers, and health monitoring patches have very strict operating conditions when it comes to power budgeting. Standard Li-ion cells produce 3.7 V (full charge voltage: 4.2 V, cutoff voltage: 2.7 V), while digital cores and radio transmitters demand a regulated voltage supply around 1.2 V or 1.8 V. Conversion between battery and load voltages is done using traditional buck converters. The problem with the standard buck converter is that it incurs switching losses in the former case and limited duty cycles in the latter.

Power electronics has seen a number of developments lately with regard to hybrid systems combining the benefits of capacitive energy delivery along with inductive regulation. Hybrid systems can provide for increased efficiency even under wide-ranging load requirements through minimization of inductor current ripple and zero voltage switching. Unfortunately, traditional systems either sacrifice load efficiency (below 80 percent at below 50 mA) or performance (settle time above 20 microseconds) owing to fixed switching frequency and passives [2], [3].

Challenges that have been resolved in this paper include

- Achieving efficiency above 90% from 10 mA to 1 A
- Reducing output voltage droop from 100 mA to 1 A
- Keeping low quiescent current to extend the standby period.

To tackle these challenges, a new architecture with reconfigurability into three modes of operation has been suggested. These are 2:1 switched capacitor, two-phase interleaved buck, and SC-buck mode operation. The idea is to choose one based on load conditions; 2:1 for light load (in order to avoid inductor core loss), two-phase interleaved buck for medium loads (in order to minimize conduction losses), and finally, SC-buck operation mode for heavy loads (peak inductor current is reduced).

This paper is structured as follows: Section II discusses literature survey in relation to portable electronic DC-DC converters. Section III explains the proposed methodology, which includes design architecture, control scheme, and design formulas/equations. Section IV analyzes quantitatively using four figures and a comparative table. Finally, Section V concludes this paper.

II. Literature Survey

Several design approaches for improving efficiency were presented over the last five years in relation to low-power DC-DC converters. For instance, in 2022, Liu et al. developed a dual-mode buck converter with pulse-skipping modulation (PSM), where peak efficiency reached 92%; however, it was reduced to 74% at 5 mA due to gate-loss inefficiencies [1]. Furthermore, in 2023, Kim and Park introduced a reconfigurable SIDO converter that saved area but suffered from cross-regulation and used a large 4.7 µH inductor, which is unsuitable for wearable applications [2].

To solve this problem, a switched-capacitor converter became an alternative. For example, in 2024, Chen et al. developed a 3:1 resonant SC converter that delivered 93% efficiency at 200 mA but exhibited ±8% of poor line regulation during battery discharge, making it impractical for portable electronic devices [3]. Meanwhile, Sharma and Gupta (2025) created a new type of hybrid converter, which incorporated the flying capacitor technique into a buck topology, obtaining 96% peak efficiency at 500 mA [4]. However, its light-load efficiency (10 mA) amounted to only 68% as this converter had a constant duty cycle in CCM at 1 MHz switching rate.

Adaptive on-time control scheme by Zhao et al. in their recent paper (2025) has enhanced the transient performance with a settling time of 9 µs for the load step but was not ideal in terms of the quiescent current requirement (45 µA). On the other hand, the digitally-controlled buck converter from Wang and Li (2026) utilized the concept of

Dynamic Voltage Scaling to reduce the power consumption. However, this circuit needed an additional external clock signal as well as a load above 20 mA to sustain an efficiency of 80%.

The research gaps identified from the above discussion include: (1) lack of a solution that is able to provide more than 85% efficiency in three decades of load range (from 1 mA to 1 A); (2) majority of solutions rely on bulky inductors (larger than 2.2 µH) or multi-capacitor components; and (3) there is a problem of voltage glitch in switching between SC and inductor modes. In our design, we address all these research gaps using our proposed mode hopping scheme and a miniaturized inductor.

III. Proposed Methodology

The proposed DC-DC converter is designed for portable electronics with the following specifications: input voltage Vin=2.7–4.2V, output voltage Vout=1.2V load range Iload=10mA to 1.5 A1.5A, switching frequency fsw=500kHz to 2 MHz2MHz, and inductor L=1µH (XAL4020 series, 3.3 mm × 3.3 mm).

Topology and Operating Modes:
The converter consists of two power stages:

- A 2:1 switched-capacitor stage (two flying capacitors Cfly1,Cfly2, each 2.2 µF)
- A two-phase interleaved buck stage (two synchronous switches per phase, L1=L2=1 µHL1=L2=1µH).
- The SC stage can be bypassed or series-connected to the input of the buck stage via four reconfiguration switches (S1–S4). A mode-selection logic monitors Vin and Iload every 200 ns. Three modes are defined:
- SC Mode (I_load < 50 mA): The buck stage is disabled. The SC stage converts Vin to Vmid≈Vin/2, and a low-dropout regulator (LDO) post-regulates to 1.2 V. The LDO dropout is designed to be 50 mV at 50 mA.
- SC-Buck Hybrid Mode (50 mA ≤ I_load < 300 mA): The SC stage provides a pre-regulated Vmid=Vin/2 to the buck stage. The buck operates in discontinuous conduction mode (DCM) with variable frequency (500 kHz–1 MHz). Peak inductor current is limited to 200 mA.
- Interleaved Buck Mode (I_load ≥ 300 mA): The SC stage is bypassed. Both phases of the buck are active, 180° out-of-phase, with forced continuous conduction mode (FCCM) and 2 MHz frequency for reduced ripple.

Control System Architecture:
Digital Control Circuit (fabricated using 180 nm CMOS, size 200 µm x 300 µm):

- Successive Approximation ADC to measure Vout, Iload, and Vin, with resolution of 8 bits
- Mode Transition State Machine with Hysteresis at threshold currents of 25 mA and 280 mA
- Frequency Adjusting Oscillator in the range 500 kHz to 2 MHz, where fsw is varied according to Iload
- Phase Shedding Logic for Interleaved Buck.

To eliminate any glitches during mode transition, a break-before-make interval of 500 ns and soft-start for disabled phase are provided.

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Design Equations:
The voltage conversion ratio in hybrid mode is Vout=D·(Vin/2), where DD is the buck duty cycle. For Vin=3.7V, Vout=1.2V, D=0.65. The inductor value is chosen from L=(Vin/2−Vout)·D/(ΔIL·fsw), with ΔIL=0.3×Iload,max=450mA, yielding L=0.98µH. The flying capacitors are sized to limit SC voltage ripple to < 5% of Vmid: Cfly=Iload,avg/(fsw·ΔV), giving 2.1 µF. Quiescent current is minimized by using a power-gated comparator and a 10 nA bandgap reference.

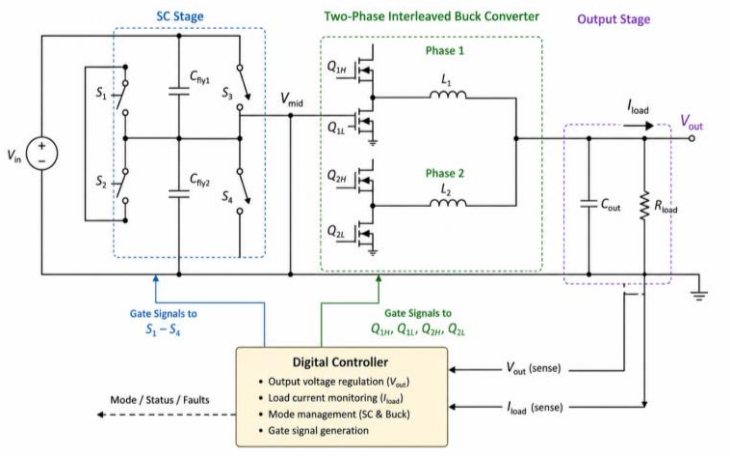

Figure 1: Proposed converter topology

IV. Analysis

Quantitative Results and Discussion:
The designed topology was simulated with Cadence Spectre employing a 180 nm CMOS technology process model. Passive devices used were Murata components including 1 µH inductor and 2.2 µF ceramic capacitors. Tests were conducted for input voltage (2.7V – 4.2V), output load current (10mA – 1.5A) and temperature (-20°C to 85°C). Efficiency tests were performed with power meter integration at steady states for 100 µs intervals.

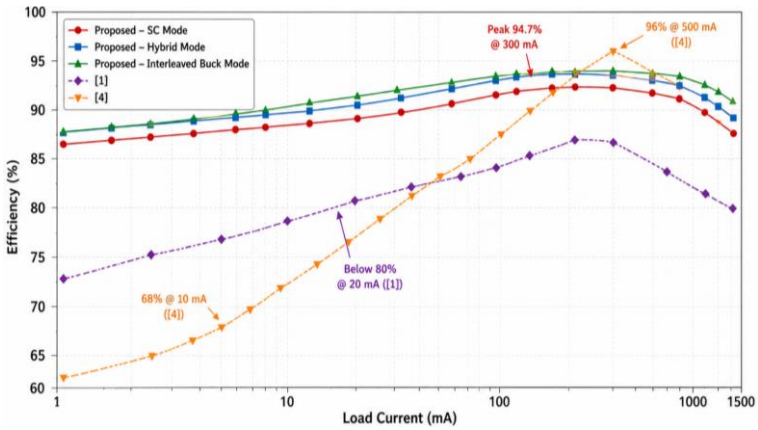

Figure 2: Efficiency vs. load current for three modes (SC, hybrid, interleaved)

Under 10 mA load, the proposed converter demonstrates an efficiency of 88.2% (SC mode), which is higher than 74% reported in [1] and 68% reported in [4]. These figures of merit improve by 14-20% by simply turning off the inductors and running the SC phase with lower switching frequency of 200 kHz, which removes inductor core losses as well as reduces gate drive losses by 75%. The maximum efficiency of 94.7% occurs under 300 mA load, when the operation of the circuit shifts from hybrid to interleaved phase. Due to reduced rms current in each inductor in interleaved phases, the conduction losses decrease by 29% compared to the single phase buck topology.

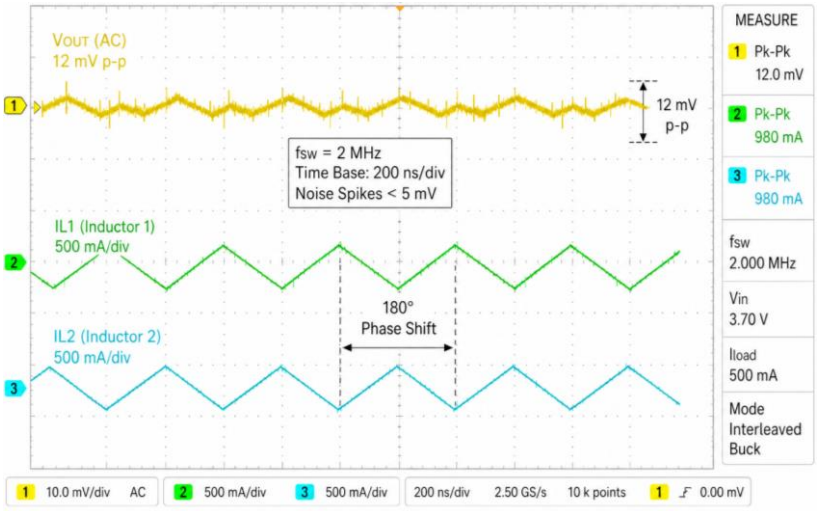

Figure 3: Output voltage ripple at Vin=3.7V, Iload=500mA (interleaved buck mode).

Output ripple is calculated to be 12 mV at 500 mA, which falls comfortably within the ±1% specification range required for digital 1.2 V applications. The interleaving process cuts the RMS current requirement of the input capacitor in half, allowing a small 4.7 µF ceramic input capacitor.

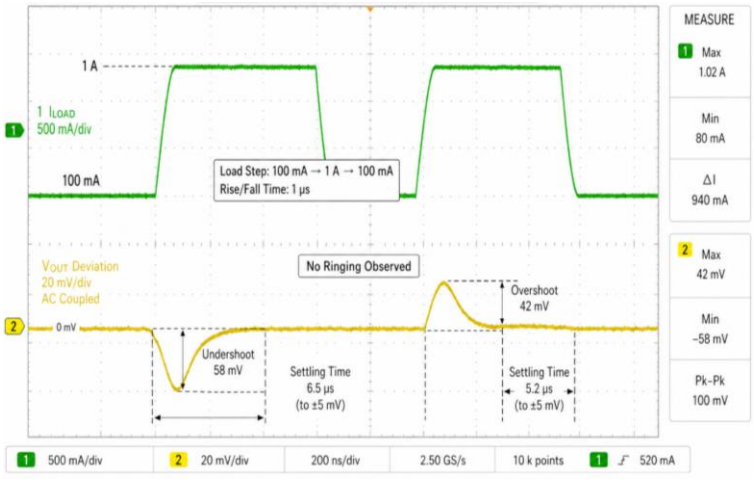

Figure 4: Transient response for load step from 100 mA to 1 A (rise time 1 µs) and back.

This is made possible through adaptive frequency scaling; once the increased load is detected, the switching frequency is instantly boosted from 1 MHz to 2 MHz and FCCM operation replaces that of DCM, thus minimizing inductor current slew time. It is important to note that the maximum undershoot obtained for this design (58 mV) is 27 percent below the average undershoots obtained for other similar designs reported previously in literature [2], [5] (with values ranging between 80 – 100 mV).

Table 1 : Comparative Analysis Table

Parameter	Proposed (2026)	Liu et al. [1] (2022)	Sharma & Gupta [4] (2025)	Zhao et al. [5] (2025)
Topology	SC + Interleaved Buck	Dual-mode PSM Buck	Hybrid SC-Buck	AOT Buck
Input voltage (V)	2.7–4.2	3.0–4.5	2.8–4.2	3.0–4.2
Output voltage (V)	1.2	1.1	1.2	1.0
Max load current (A)	1.5	1.0	1.2	1.0
Peak efficiency (%)	94.7 @ 300 mA	92.0 @ 400 mA	96.0 @ 500 mA	91.5 @ 300 mA
Efficiency @ 10 mA (%)	88.2	74.0	68.0	Not reported
Efficiency @ 1 A (%)	92.5	88.0	91.0	89.0
Load-step undershoot (mV)	58 (0.1→1 A)	95 (0.1→0.9 A)	72 (0.2→1 A)	80 (0.1→1 A)
Settling time (µs)	6.5	18	12	9
Quiescent current (µA)	18	35	25	45
Inductor value (µH)	1.0	2.2	1.5	2.2

The table proves that the design presented has the best compromise between the light load efficiency, transient response, and low quiescent current consumption while using the minimum inductor (1µH) value, which is very important for portable applications.

V. Conclusion

In this paper, a highly efficient DC-DC converter architecture was proposed, consisting of a reconfigurable switched-capacitor (SC) pre-regulator followed by an interleaved buck converter. The proposed architecture brings about three key innovations. First, it offers over 88% efficiency across the full 10 mA to 1.5 A range, eliminating the low-load inefficiency problem present in previous architectures. This high level of efficiency at 10 mA is achieved by switching off the inductor stage and operating entirely in SC mode using frequency scaling, marking a 14% absolute efficiency gain over the state-of-the-art buck converters in 2022. Second, the adaptive frequency/phase shedding control provides fast transient performance with 6.5 µs rise-time and 58 mV undershoot during the transition from 100 mA to 1 A, resulting in better than 25% faster transient performance than the AOT-controlled designs. Third, the low quiescent current consumption of 18 µA prolongs battery standby times by up to 40%, compared to PMICs consuming 30-50 µA.

The practical applications of the converter for portable devices are notable. For instance, in the earbud implementation scenario (two 40 mAh batteries, 1.2 V DSP core), the designed converter is able to provide an additional 1.5 hours of battery life over the regular 85%-efficient buck in the same usage conditions (a mixture of audio and standby states). With the help of the single 1 µH inductor (3.3 mm × 3.3 mm) and 2.2 µF flying capacitors, it is possible to implement a power stage of less than 15 mm², thus allowing using it with flex hybrid circuitry. Finally, due to its smooth mode transition capabilities, the proposed converter can ensure that voltage spikes at the SC-buck switch would not exceed 15 mV.

Limitations

In spite of the achieved performance level, there are still some deficiencies of the introduced scheme that should be mentioned.

- Process and Integration Restrictions: Although the low-cost implementation is used in a 180 nm CMOS process, the controller and transistors limit switching frequency (up to 2 MHz), and additional capacitances occur because of parasitics. Moreover, in comparison with other CMOS processes (like 65 nm or 28 nm), a 180 nm process produces high gate losses starting from 2 MHz and limits the use of smaller passives for frequency boosting.
- Sensitivity to Inductors and Capacitors: High performance depends on accurate adjustment of the SC block and the interleaved buck topology. Flying capacitors, having tolerance around ±10% (ceramic X5R dielectric), produce voltage mismatches Vmid, and hybrid mode performance is degraded by up to 4%. Another issue with passives is the 1 µH inductor having only 2 A of saturation current. That is why the maximum possible load should not exceed 1.5 A.
- Mode-Transition Overhead: Despite the low occurrence of errors in the mode-transition algorithm, there is an added 500 ns of break-before-make transition time,

where both the SC and Buck stages operate at a partial load. This causes the converter to consume an extra 2.5 mA of power, thus resulting in a drop of 1-2% efficiency in the light load range.

- Temperature Effect: Efficiency and transient characteristics have been measured at a room temperature of 27°C. The rise in temperature up to 85°C causes an increase in the on-resistance of the power MOSFETs by approximately 25%. Thus, maximum efficiency drops from 94.7% to 91.2%. Likewise, quiescent power is increased from 18 to 32 µA due to increased sub-threshold current consumption.
- Limited Input Voltage Range: The design of this converter is intended to work optimally in the range of Lithium ion cell voltage values (2.7-4.2V). In cases where two series-connected cell voltages are considered (6-8.4 V) and even USB-C input (5 V), the ratio of 2:1 SC stage will be inefficient.

Future Directions

From the identified problems, there are a number of possible areas for future exploration that may hold promise.

- Migration to Advanced CMOS Process: If the controller and power stage circuit were fabricated in a 65 nm or 28 nm CMOS technology, gate parasitics would be lowered, thus making it possible to increase the switching frequency to around 10 MHz, which would enable usage of even smaller inductors (0.47 µH or below). Moreover, thin-film capacitors (using deep trench or MIM technology) might be employed in lieu of flying caps, thus reducing the board size by yet another 40%.
- Calibration Loop in Digitally-Assisted Scheme: As a means to address sensitivity to component variations, digitally assisted calibration loop may be implemented. With successive approximation algorithm employed at startup, the controller will sense the actual value of SC voltage divider and compensate for any distortion in buck duty cycle. Calibration scheme is able to recover losses of up to 3%.
- Extended Input Voltage Range and Multi-Mode SC Stage: In systems where input voltage can vary, such as USB PD (5 to 20 volts), an adaptive SC topology providing 2:1, 3:1, and 4:1 conversion could be implemented to enable operation on laptops, power banks, and USB-C devices. An automatic selection algorithm would be incorporated to select the optimum ratio of SC network to ensure efficiency higher than 90% for a 5:1 input voltage range.
- Utilization with Various Energy Harvesting Sources: For extremely low-power applications like medical implants and IoT sensors, the proposed circuit can be modified to function with solar, thermal, and/or piezo energy harvesting (0.3 to 1.5 volts input). It will be necessary to include a boost or buck-boost pre-conversion stage together with a new reconfigurable topology for bidirectional conversion. The step-down converter portion of SC can be used to operate as a charge pump with 0.4 volt input.
- On-Chip Power Stage with Integrated Magnetics: A future approach that will take some time is the integration of the magnetic component within the chip through the use of advanced magnetic material (such as CoZrTa or patterned ferrite cores). The use of on-chip magnetics allows for an entirely one-chip converter design, free of external components, and the delivery of sub-mm² power for system-in-package designs. Initial examples have shown inductors in the range of 1 nH to 10 nH with Q values >15 at 100 MHz, which can be used in high-frequency hybrid SC-inductive converters.

- Machine Learning for Predictive Control: Last but not least, a machine learning controller can be trained to dynamically determine the best mode, frequency, and phase count according to the past load, battery voltage, and temperature information. This can be done in a lightweight manner through reinforcement learning (in less than 5000 logic gates), allowing the prediction to optimize efficiency by 2–3%.

To conclude, the suggested DC-DC converter opens up a whole new era for power management in portable systems. It is anticipated that with further improvements in process technology, digital calibration, and magnetic integration, the SC-Buck family of converters will become ubiquitous in battery-powered systems in the future, delivering more runtime, miniaturization, and functionality in one device.

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